DOT1	WS	REP 1	DOT	WS	REP 2	DOT	WS	REP 3	DOT	WS	REP 4	DOT	WS	REP 5	DOT	WS	REP 6	DOT
101 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit

WS	REP 7	DOT	WS	REP 8	DOT	WS	REP 9	DOT	WS	REP 10	DOT	WS	REP 11	.....
11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	37 bit	11 bit	40 bit	

FIG. 1

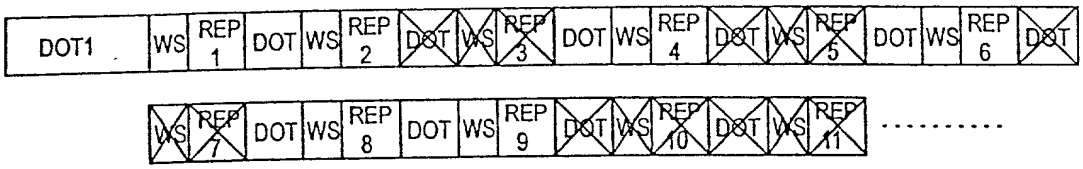

FIG. 2a

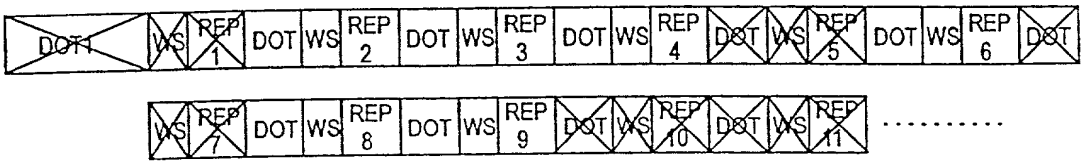

FIG. 2b

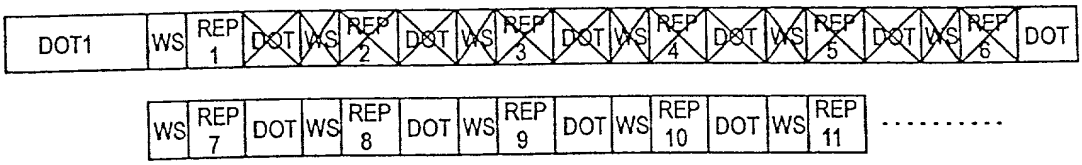

FIG. 2c

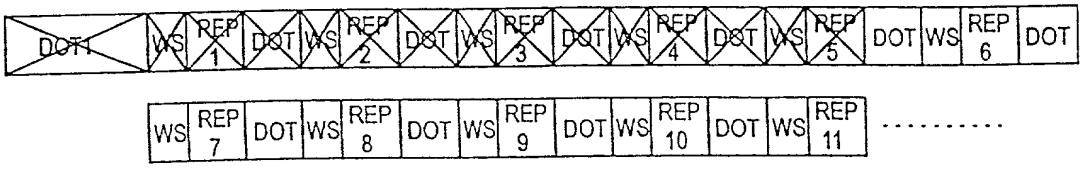

FIG. 2d

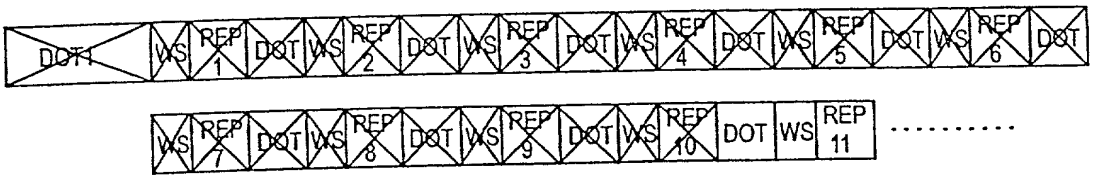

FIG. 3a

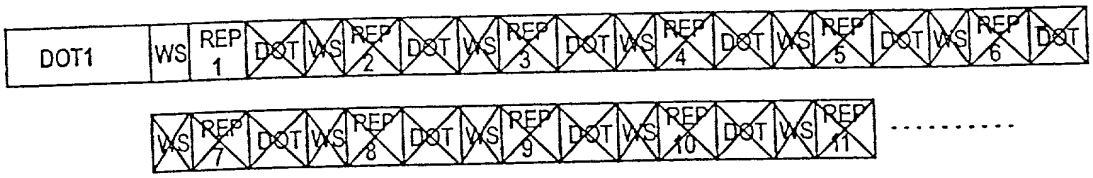

FIG. 3b

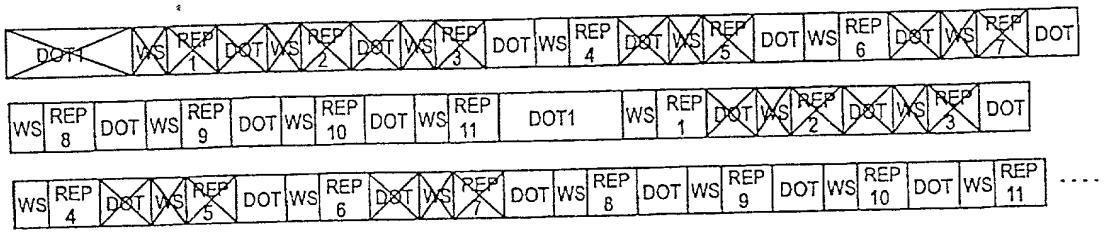

FIG. 4a

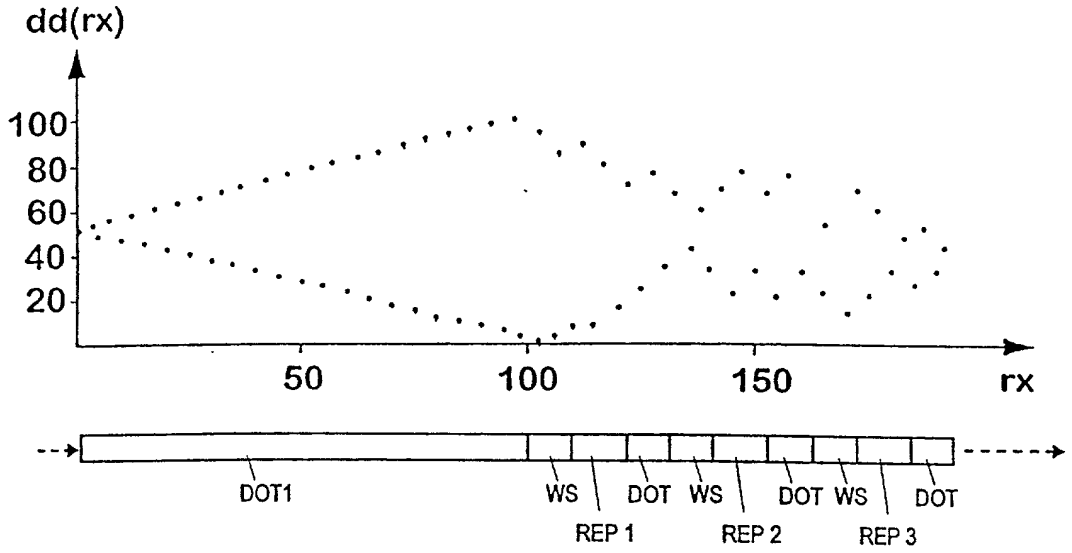
dd(rx)
100
80
60
40
20
50
100
150
rx
DOT1
WS
DOT
WS
DOT
WS
DOT
REP 1
REP 2
REP 3

FIG. 4b

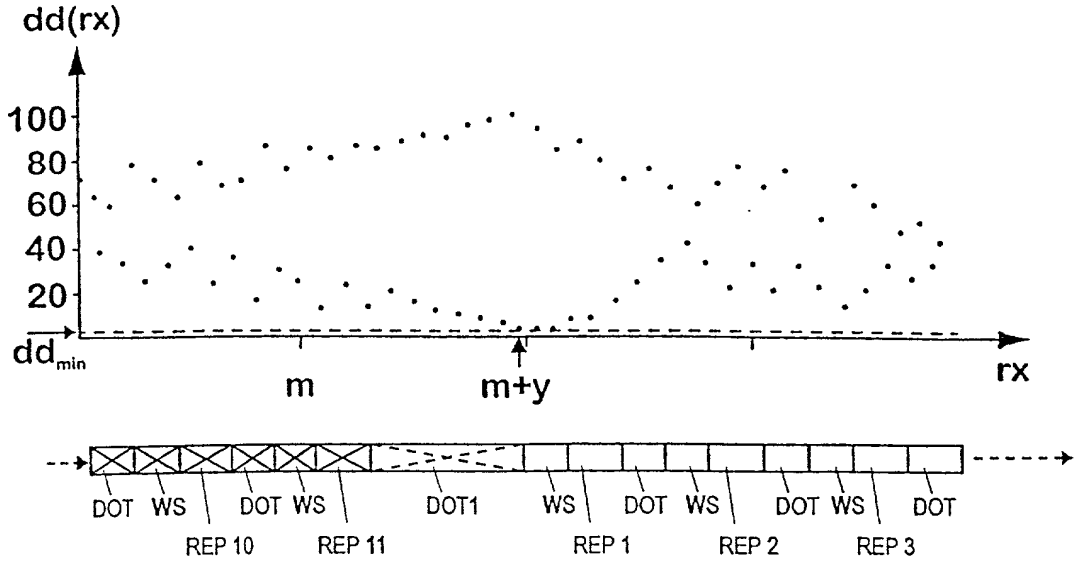
dd(rx)
100
80
60
40
20
dd$_{min}$
m
m+y
rx
DOT
WS
DOT
WS
DOT1
WS
DOT
WS
DOT
WS
DOT
REP 10
REP 11
REP 1
REP 2
REP 3

FIG. 4c

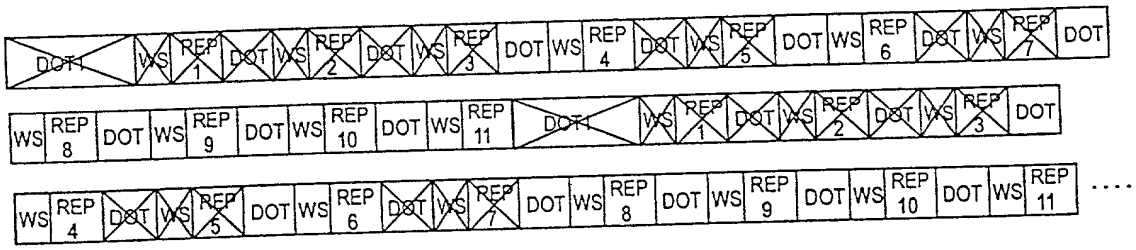
DOT WS REP 1 DOT WS REP 2 DOT WS REP 3 DOT WS REP 4 DOT WS REP 5 DOT WS REP 6 DOT WS REP 7 DOT
WS REP 8 DOT WS REP 9 DOT WS REP 10 DOT WS REP 11 DOT WS REP 1 DOT WS REP 2 DOT WS REP 3 DOT
WS REP 4 DOT WS REP 5 DOT WS REP 6 DOT WS REP 7 DOT WS REP 8 DOT WS REP 9 DOT WS REP 10 DOT WS REP 11 ....

FIG. 4d

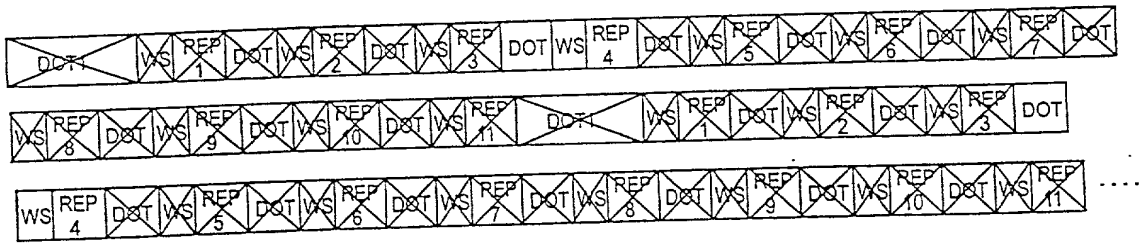
DOT WS REP 1 DOT WS REP 2 DOT WS REP 3 DOT WS REP 4 DOT WS REP 5 DOT WS REP 6 DOT WS REP 7 DOT
WS REP 8 DOT WS REP 9 DOT WS REP 10 DOT WS REP 11 DOT WS REP 1 DOT WS REP 2 DOT WS REP 3 DOT
WS REP 4 DOT WS REP 5 DOT WS REP 6 DOT WS REP 7 DOT WS REP 8 DOT WS REP 9 DOT WS REP 10 DOT WS REP 11 ....

FIG. 5